

## CLAIMS

## 1. A step-up apparatus comprising:

5 a first level shift circuit for receiving a first clock signal to generate two phase-opposite second clock signals;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

10 a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate a positive voltage; and

15 a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said positive voltage,

20 a high level of said second clock signals being not higher than said positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signals being not higher than said power supply voltage,

25 a low level of said third clock signals being not lower than said negative voltage.

2. The step-up apparatus as set forth in claim 1, wherein said first level shift circuit comprises:

30 first and second cross-coupled load P-channel MOS transistors whose sources receive said positive voltage; and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first

and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

3. The step-up apparatus as set forth in claim 1, wherein said second level shift circuit comprises:

10 first and second cross-coupled N-channel Load MOS transistors whose sources receive said voltage at said ground terminal; and

15 third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

20 gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second P-channel drive MOS transistors generating said third clock signals.

4. The step-up apparatus as set forth in claim 1, wherein said change pump circuit comprises:

25 a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

30 an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging

capacitor and said second charging switching element for generating an "i" times said power supply voltage.

5. The step-up apparatus as set forth in claim 4, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

                  said first charging switching element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

10              said second charging switching element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

6. The step-up apparatus as set forth in claim 1, wherein said charge pump circuit steps up said power supply voltage further using said third clock signals, said pump circuit comprising:

                  a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

20              an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

                  said first step-up switching element comprising a P-channel MOS transistor controlled by one of said third clock signals,

                  said second charging switching element of said 2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

said first charging switching element of said i-th (i= 2, 3, ...) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

5            said second charging switching element of said i-th (i= 3, 4, ...) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

10            said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal.

7.    A step-up apparatus comprising:

                  a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

15            a second level shift circuit for receiving said first clock signal to generate a third clock signal;

                  a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate a positive voltage; and

20            a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said positive voltage,

25            a high level of said second clock signals being not higher than said positive voltage,

                  a low level of said second clock signals being not lower than a voltage at a ground terminal,

30            a high level of said third clock signal being not higher than said voltage at said ground voltage,

                  a low level of said third clock signal being not lower than said negative voltage.

8. The step-up apparatus as set forth in claim 7, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said positive voltage;

5 and

first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

10 gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

15 9. The step-up apparatus as set forth in claim 7, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting said first clock signal;

20 first and second cross-coupled N-channel Load MOS transistors whose sources receive said negative voltage; and

25 third and second P-channel drive MOS transistors whose sources receive said voltage at said ground terminal and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving an output signal of said polarity inverting circuit and its inverted signal, respectively,

30 the drain of one of said first and second P-channel drive MOS transistors generating said third clock signal.

10. The step-up apparatus as set forth in claim 9,

wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

11. The step-up apparatus as set forth in claim 7,  
5 wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and  
10 an i-th ( $i=2, 3, \dots, K$ ) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging 15 capacitor and said second charging switching element for generating an "i" times said power supply voltage.

12. The step-up apparatus as set forth in claim 11,  
wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by  
20 one of said second clock signals,

said first charging switching element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

25 said second charging switching element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

13. A step-up apparatus comprising:

a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock 30 signals;

a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

5 a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages, said first positive voltage being smaller than said second positive voltage; and

10 a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said second positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said second positive voltage,

15 a high level of said second clock signals being not higher than said second positive voltage,

20 a low level of said second clock signals being not lower than a voltage at a ground terminal,

25 a high level of said third clock signals being not higher than said power supply voltage,

30 a low level of said third clock signals being not lower than said negative voltage.

14. The step-up apparatus as set forth in claim 13, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said second positive voltage; and

25 first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

30 gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

15. The step-up apparatus as set forth in claim 13, wherein said second level shift circuit comprises:

first and second cross-coupled N-channel load MOS transistors whose sources receive said voltage as said 5 ground terminal; and

third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, 10 respectively,

gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second P-channel 15 drive MOS transistors generating said third clock signals.

16. The step-up apparatus as set forth in claim 13, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage 20 terminal, for generating said power supply voltage; and

an i-th ( $i=2, 3, \dots, K$ ) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said 25 charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

said L-th ( $L=2, 3, \dots, K-1$ ) circuit generating 30 said first positive voltage,

said K-th ( $K > L$ ) circuit generating said second positive voltage.

17. The step-up apparatus as set forth in claim 16,

wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

5                   said first charging switching element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

                  said second charging switching element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

10           18. The step-up apparatus as set forth in claim 13, wherein said charge pump circuit steps up said power supply voltage further using said third clock signals, pump circuit comprising:

15           a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

20           an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

25           said first step-up switching element comprising a P-channel MOS transistor controlled by one of said third clock signals,

                 said second charging switching element of said 2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

                 said first charging switching element of said i-th (i= 2, 3, ..., K) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging switching element of said i-th (i= 3, 4, ..., K) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

5                  said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal,

                  said L-th (L=2, 3, ..., K-1) circuit generating said first positive voltage,

10                said K-th (K > L) circuit generating said second positive voltage.

19. A step-up apparatus comprising:

                  a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

                  a second level shift circuit for receiving said first clock signal to generate a third clock signal;

20                a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages; and

                  a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said second positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said second positive voltage,

                  a high level of said second clock signals being not higher than said second positive voltage,

30                a low level of said second clock signals being not lower than a voltage at a ground terminal,

                  a high level of said third clock signal being not higher than said voltage at said ground voltage,

                  a low level of said third clock signal being

not lower than said negative voltage.

20. The step-up apparatus as set forth in claim 19, wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel  
5 MOS transistors whose sources receive said second positive  
voltage; and

first and second N-channel drive MOS  
transistors whose drains are connected to drains of said first  
and second cross-coupled load P-channel MOS transistors,  
10 respectively,

gates of said first and second N-channel drive  
MOS transistors receiving said first clock signal and its  
inverted signal, respectively,

the drains of said first and second N-channel  
15 drive MOS transistors generating said second clock signals.

21. The step-up apparatus as set forth in claim 19, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting  
said first clock signal;

20 first and second cross-coupled N-channel Load  
MOS transistors whose sources receive said negative voltage;  
and

third and second P-channel drive MOS  
transistors whose sources receive said voltage at said ground  
25 terminal and whose drains are connected to drains of said first  
and second cross-coupled load N-channel MOS transistors,  
respectively,

gates of said first and second drive P-channel  
MOS transistors receiving an output signal of said polarity  
30 inverting circuit and its inverted signal, respectively,

the drain of one of said first and second  
P-channel drive MOS transistors generating said third clock  
signal.

22. The step-up apparatus as set forth in claim 21, wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

5 23. The step-up apparatus as set forth in claim 19, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

10 an  $i$ -th ( $i=2, 3, \dots, K$ ) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and 15 a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an " $i$ " times said power supply voltage,

said  $L$ -th ( $L=2, 3, \dots$ ) circuit generating said first positive voltage,

20 said  $K$ -th ( $K > L$ ) circuit generating said second positive voltage,

24. The step-up apparatus as set forth in claim 23, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by 25 one of said second clock signals,

said first charging switching element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

30 said second charging switching element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

25. A step-up apparatus comprising:

a first level shift circuit for receiving a

clock first signal to generate two phase-opposite second clock signals;

5 a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

10 a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages, said first positive voltage being smaller than said second positive voltage; and

15 a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said first positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said first positive voltage,

20 a high level of said second clock signals being not higher than said first positive voltage,

25 a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signals being not higher than said power supply voltage,

a low level of said third clock signals being not lower than said negative voltage.

26. The step-up apparatus as set forth in claim 25,

wherein said first level shift circuit comprises:

first and second cross-coupled load P-channel MOS transistors whose sources receive said first positive voltage; and

30 first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

5 the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

27. The step-up apparatus as set forth in claim 25, wherein said second level shift circuit comprises:

10 first and second cross-coupled N-channel Load MOS transistors whose sources receive said voltage as said ground terminal; and

15 third and second P-channel drive MOS transistors whose sources receive said power supply voltage and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel MOS transistors receiving said first clock signal and its inverted signal, respectively,

20 the drains of said first and second P-channel drive MOS transistors generating said third clock signals.

28. The step-up apparatus as set forth in claim 25, wherein said change pump circuit comprises:

25 a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

30 an i-th ( $i=2, 3, \dots, L$ ) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

said K-th ( $K=2, 3, \dots, L-1$ ) circuit generating  
said first positive voltage,

                          said L-th ( $L > K$ ) circuit generating said  
second positive voltage.

5       29. The step-up apparatus as set forth in claim 28,  
wherein each of said first and second step-up switching  
elements comprises a P-channel MOS transistor controlled by  
one of said second clock signals,

10      said first charging switching element  
comprising an N-channel MOS transistor controlled by the one  
of said second clock signals,

                          said second charging switching element  
comprising a P-channel MOS transistor controlled by the other  
of said second clock signals.

15      30. The step-up apparatus as set forth in claim 25,  
wherein said charge pump circuit steps up said power supply  
voltage further using said third clock signals, said pump  
circuit comprising:

20      a first circuit including a first step-up  
switching element, connected to said power supply voltage  
terminal, for generating said power supply voltage; and

25      an i-th ( $i=2, 3, \dots, L$ ) circuit including a  
charging capacitor, a first charging switching element  
connected between said ground terminal and said charging  
capacitor, a second charging element connected between said  
charging capacitor and said power supply voltage terminal, and  
a second step-up switching element connected to said charging  
capacitor and said second charging switching element for  
generating an "i" times said power supply voltage,

30      said first step-up switching element  
comprising a P-channel MOS transistor controlled by one of  
said third clock signals,

                          said second charging switching element of said

2-nd circuit comprising a P-channel MOS transistor controlled by the other of said third clock signals,

5                   said first charging switching element of said i-th (i= 2, 3, ..., L) circuit comprising an N-channel MOS transistor controlled by the one of said second clock signals,

                  said second charging switching element of said i-th (i= 3, 4, ..., L) circuit comprising a P-channel MOS transistor controlled by the other of said second clock signals,

10                  said second step-up switching element comprising a P-channel MOS transistor controlled by the other of said second clock signal,

                  said K-th (K=2, 3, ..., L-1) circuit generating said first positive voltage,

15                  said L-th (L > K) circuit generating said second positive voltage.

31. A step-up apparatus comprising:

20                  a first level shift circuit for receiving a clock first signal to generate two phase-opposite second clock signals;

                  a second level shift circuit for receiving said first clock signal to generate a third clock signal;

25                  a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said second clock signals to generate first and second positive voltages; and

30                  a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said first positive voltage using said third clock signal to generate a negative voltage whose absolute value is the same as said first positive voltage,

                  a high level of said second clock signals being not higher than said first positive voltage,

a low level of said second clock signals being not lower than a voltage at a ground terminal,

a high level of said third clock signal being not higher than said voltage at said ground voltage,

5 a low level of said third clock signal being not lower than said negative voltage.

32. The step-up apparatus as set forth in claim 31, wherein said first level shift circuit comprises:

10 first and second cross-coupled load P-channel MOS transistors whose sources receive said first positive voltage; and

15 first and second N-channel drive MOS transistors whose drains are connected to drains of said first and second cross-coupled load P-channel MOS transistors, respectively,

20 gates of said first and second N-channel drive MOS transistors receiving said first clock signal and its inverted signal, respectively,

the drains of said first and second N-channel drive MOS transistors generating said second clock signals.

33. The step-up apparatus as set forth in claim 31, wherein said second level shift circuit comprises:

a polarity inverting circuit for inverting said first clock signal;

25 first and second cross-coupled N-channel Load MOS transistors whose sources receive said negative voltage; and

30 third and second P-channel drive MOS transistors whose sources receive said voltage at said ground terminal and whose drains are connected to drains of said first and second cross-coupled load N-channel MOS transistors, respectively,

gates of said first and second drive P-channel

MOS transistors receiving an output signal of said polarity inverting circuit and its inverted signal, respectively, the drain of one of said first and second P-channel drive MOS transistors generating said third clock signal.

34. The step-up apparatus as set forth in claim 33, wherein said polarity inverting circuit comprises a capacitor for receiving said first clock signal and a diode between said capacitor and said ground terminal.

10 35. The step-up apparatus as set forth in claim 31, wherein said charge pump circuit comprises:

a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage; and

15 an i-th ( $i=2, 3, \dots, L$ ) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage,

20 said K-th ( $K=2, 3, \dots$ ) circuit generating said first positive voltage,

25 said L-th ( $L > K$ ) circuit generating said second positive voltage,

36. The step-up apparatus as set forth in claim 35, wherein each of said first and second step-up switching elements comprises a P-channel MOS transistor controlled by one of said second clock signals,

30 said first charging switching element comprising an N-channel MOS transistor controlled by the one of said second clock signals,

said second charging switching element comprising a P-channel MOS transistor controlled by the other of said second clock signals.

37. A step-up apparatus comprising:

5           a first level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ..., a K-th clock signal (K= 2, 3, ...) having a definite voltage swing;

10          a second level shift circuit for receiving said first clock signal to generate two phase-opposite third clock signals;

15          a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ..., K-th clock signals to generate a positive voltage; and

20          a polarity inverting circuit, connected to said charge pump circuit and said second level shift circuit, for inverting said positive voltage using said third clock signals to generate a negative voltage whose absolute value is the same as said positive voltage,

38. The step-up apparatus as set forth in claim 37, wherein said charge pump circuit comprises:

25          a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

30          an i-th (i=2, 3, ..., K) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging element for

generating an "i" times said power supply voltage.

39. The step-up apparatus as set forth in claim 38, wherein said first step-up switching element comprises a P-channel MOS transistor controlled by said first clock signal,

said first charging switching element comprising an N-channel MOS transistor controlled by said first clock signal,

10 said second charging switching element comprising an N-channel MOS transistor controlled by said second clock signal,

said second step-up switching element of said i-th ( $i = 2, 3, \dots, K$ ) circuit comprising a P-channel MOS transistor controlled by said i-th clock signal.

15 40. The step-up apparatus as set forth in claim 38, wherein said first level shift circuit comprises an i-th (i=2, 3, ..., K) level shift unit is powered by  $(i-2) \cdot V_{DD}$ ,  $(i-1) \cdot V_{DD}$  and  $i \cdot V_{DD}$  where  $V_{DD}$  is a power supply voltage.

41. The step-up apparatus as set forth in claim 40,  
20 wherein said i-th level shift unit comprises:

cross-coupled first and second load N-channel MOS transistors whose sources receive  $(i-2) \cdot V_{DD}$ ; first and second drive P-channel MOS transistors whose sources receive  $(i-1) \cdot V_{DD}$  and whose drains are connected to drains of said first and second load N-channel MOS transistors, respectively;

cross-coupled first and second load P-channel MOS transistors whose sources receive  $i \cdot V_{DD}$ ; and

first and second drive N-channel MOS  
30 transistors whose sources receive  $(i-2) \cdot V_{DD}$ , whose drains are connected to drains of said first and second load P-channel MOS transistors, respectively, and whose gates are connected to gates of said first and second load N-channel MOS

transistors, respectively,

gates of said first and drive P-channel MOS transistors receiving said (i-1)-th clock signal and its inverted signal,

5 the drain of said second drive N-channel MOS transistor generating said i-th clock signal via an inverter.

42. A step-up apparatus comprising:

10 a level shift circuit for receiving a first clock signal to generate a 2nd clock signal, a 3rd clock signal, ... , a K-th clock signal (K= 2, 3, ...) having a definite voltage swing; and

15 a charge pump circuit, connected to said first level shift circuit, for stepping up a power supply voltage at a power supply voltage terminal using said first, second, ... , K-th clock signals to generate a positive voltage.

43. The step-up apparatus as set forth in claim 42, wherein said charge pump circuit comprises:

20 a first circuit including a first step-up switching element, connected to said power supply voltage terminal, for generating said power supply voltage in accordance with said first clock signal;

25 an i-th (i=2, 3, ... , K) circuit including a charging capacitor, a first charging switching element connected between said ground terminal and said charging capacitor, a second charging element connected between said charging capacitor and said power supply voltage terminal, and a second step-up switching element connected to said charging capacitor and said second charging switching element for generating an "i" times said power supply voltage.

30 44. The step-up apparatus as set forth in claim 43, wherein said first step-up switching element comprises a P-channel MOS transistor controlled by said first clock signal,

said first charging switching element comprising an N-channel MOS transistor controlled by said first clock signal,

5                  said second charging switching element comprising an N-channel MOS transistor controlled by said second clock signal,

                  said second step-up switching element of said i-th ( $i = 2, 3, \dots, K$ ) circuit comprising a P-channel MOS transistor controlled by said i-th clock signal.

10              45. The step-up apparatus as set forth in claim 43, wherein said level shift circuit comprises an i-th ( $i = 2, 3, \dots, K$ ) level shift unit is powered by  $(i-2) \cdot V_{DD}$ ,  $(i-1) \cdot V_{DD}$  and  $i \cdot V_{DD}$  where  $V_{DD}$  is a power supply voltage.

15              46. The step-up apparatus as set forth in claim 45, wherein said i-th level shift unit comprises:

                  cross-coupled first and second load N-channel MOS transistors whose sources receive  $(i-2) \cdot V_{DD}$ ;

20              first and second drive P-channel MOS transistors whose sources receive  $(i-1) \cdot V_{DD}$  and whose drains are connected to drains of said first and second load N-channel MOS transistors, respectively;

                  cross-coupled first and second load P-channel MOS transistors whose sources receive  $i \cdot V_{DD}$ ; and

25              first and second drive N-channel MOS transistors whose sources receive  $(i-2) \cdot V_{DD}$ , whose drains are connected to drains of said first and second load P-channel MOS transistors, respectively, and whose gates are connected to gates of said first and second load N-channel MOS transistors, respectively,

30              gates of said first and drive P-channel MOS transistors receiving said  $(i-1)$ -th clock signal and its inverted signal,

                  the drain of said second drive N-channel MOS

transistor generating said i-th clock signal via an inverter.